Amendments to the Claims

1. (CURRENTLY AMENDED) Method of performing access to a single-port memory device ~~(13)~~, the method comprising the steps of:

- providing a memory access device ~~(15, 30)~~ to control the access,
- processing a first access-signal (WEN) of high priority at a first clock rate,
- processing a second access-signal (REBL) of low priority at a second clock rate,

wherein the first clock rate exceeds the second clock rate,

- providing direct access to the memory device ~~(13)~~ for the first access-signal (WEN) of high priority, and
- properly delaying the first access-signal (WEN) of high priority to generate an access-timing according to the demands of the memory device ~~(13)~~.

2. (CURRENTLY AMENDED) Method according to claim 1, characterized in that access to the memory device ~~(13)~~ for the second access-signal (REBL) of low priority is generally provided, except in the case that an access of a first access-signal (WEN) of high priority is in preparation and/or in process, to guarantee direct access to the memory device ~~(13)~~ for the first access-signal (WEN) of high priority.

3. (CURRENTLY AMENDED) Method according to ~~claim 1 or 2~~claim 1, characterized in that in the case that access to the memory device ~~(13)~~ is not provided for the second access-signal (REBL) of low priority, the second access-signal (REBL) is backed up.

4. (CURRENTLY AMENDED) Method according to one of ~~claims 1 to 3~~claim 1, characterized in that in the case that access to the memory device ~~(13)~~ is not provided for the second access-signal (REBL) of low priority, direct access to the memory device ~~(13)~~ is made by the first access-signal (WEN) of high priority and/or after completion of an access to the memory device ~~(13)~~ by the first access-signal (WEN) of high priority access ~~(15)~~ is made by the second access-signal of low priority.

5. (ORIGINAL) Method according to claim 4, characterized in that the completion of the access made by the first access-signal (WEN) of high priority is used to introduce the access of the second access-signal (REBL) of low priority.

6. (CURRENTLY AMENDED) Method according to one of ~~claims 1 to 5~~claim 1, characterized in that the proper delay of the first access-signal (WEN) of high priority is available from a number of delay periods (t_0, t_1, t_2, t_3) offered for choice to generate an access-timing according to the demands of the memory device ~~(13)~~.

7. (CURRENTLY AMENDED) Method according to one of ~~claims 1 to 6~~claim 1, characterized in that a time gap in between two subsequent accesses of first access-signals (WEN) of high priority is sufficiently wide to complete an access of a second access-signal of low priority (REBL) therein.

8. (CURRENTLY AMENDED) Method according to one of ~~claims 1 to 7~~claim 1, characterized in that the first access-signal (WEN) of high priority is a write-signal (WEN), in particular a write-enable signal (WEN) and/or the second access-signal (REBL) of low priority is a read-signal (REBL), in particular a read-enable signal (REBL).

9. (CURRENTLY AMENDED) Method according to one of the ~~claims 1 to 8~~claim 1, characterized in that the first clock rate is an external clock rate of the memory access device and/or the second clock rate is an internal clock rate (RAM-CLK) of the memory access device.

10. (CURRENTLY AMENDED) Memory access device ~~(15, 30)~~ for performing controlled access to a single-port memory device ~~(13)~~, comprising:

- a first path for processing a first access-signal (WEN) of high priority at a first clock rate,

- a second path for processing a second access-signal (REBL) of low priority at a second clock rate, wherein the first clock rate exceeds the second clock rate,
- a control-assembly ~~(31)~~ for providing direct access to the memory device ~~(13)~~ for the first access-signal (WEN) of high priority,
- a delay-assembly ~~(32)~~ for properly delaying (t_0, t_1, t_2, t_3) the first access-signal (WEN) of high priority adapted to generate an access-timing according to the demands of the memory device ~~(13)~~.

11. (CURRENTLY AMENDED) Memory access device ~~(15, 30)~~ according to claim 10, characterized in that the first and/or second path comprises a number of control elements, in particular a logic gate and/or a flip-flop, functionally connected with each other and an input-interface and an output-interface.

12. (CURRENTLY AMENDED) Memory access device ~~(15, 30)~~ according to ~~claim 10 or 11~~claim 10, characterized in that at least the second path comprises a storage element to perform a back-up function.

13. (CURRENTLY AMENDED) Memory access device ~~(15, 30)~~ according to one of the ~~claim 10 to 12~~claim 10, characterized in that the control-assembly ~~(31)~~ comprises at least one input-interface delay-assembly-signal and/or access-addresses and an output-interfaces to transmit an address-signal and/or a RAM-select signal.

14. (CURRENTLY AMENDED) Memory access device ~~(15, 30)~~ according to one of ~~claims 10 to 13~~claim 10, characterized in that the delay-assembly ~~(32)~~ comprises a number of resistance-capacitor elements and/or buffer elements, in particular a chain ~~(40)~~ thereof.

15. (CURRENTLY AMENDED) Memory access device ~~(15, 30)~~ according to one of ~~claims 10 to 14~~claim 10, characterized by a single external clock-rate input.

16. (CURRENTLY AMENDED) Integrated circuit device ~~(10)~~ comprising:
- a single-port memory device ~~(13)~~,

- a means for supplying a first clock rate,
- a single external-clock-rate input ~~(18)~~ for supplying a second clock rate, and
- a memory access device ~~(15)~~ of one of the ~~claims 10 to 15~~claim 10 for accessing the single-port memory device ~~(13)~~.

17. (CURRENTLY AMENDED) Integrated circuit device ~~(10)~~ according to claim 16, wherein the means for supplying a first clock rate comprises an internal timing controller ~~(9)~~.

18. (CURRENTLY AMENDED) Integrated circuit device ~~(10)~~ according to claim 16, characterized by comprising a number of single-port memory devices ~~(13)~~, each one of the number of single-port memory devices ~~(13)~~ being addressable separately and/or a number of memory access devices ~~(15)~~ each one of the number of single-port memory devices ~~(13)~~ being related to one of the number of memory access devices ~~(15)~~, wherein in particular the number of memory access devices ~~(15)~~ are identical to each other.

19. (CURRENTLY AMENDED) Method of use of an integrated circuit device ~~(10)~~, in particular of an integrated circuit device as claimed in ~~claims 16 or 17~~claim 16, as an application specific integrated circuit device ~~(10)~~, in particular for accessing a display device ~~(12)~~, in particular for use with regard to a display driver.